In the Claims:

1. (Currently Amended) A data processor comprising:

a) at least one off-core execution unit;

b) a CLIW memory for storing at least one Configurable Long Instruction Word (CLIW) instruction; and

c) a core processor operative to retrieve said at least one CLIW instruction from said CLIW memory and forward at least a respective portion of said at least one CLIW instruction to at least one of said at least one off-core execution units;

wherein each said off-core execution unit is an external off-core processing unit connected to said core processor in an interchangeable and selectable manner by means of an interface.

2. (Original) The data processor of claim 1, wherein said core processor is operative to execute a plurality of instructions of an instruction set, and wherein said instruction set includes a Reference Instruction for initiating retrieval and execution of said CLIW instruction.

3. (Original) The data processor of claim 1, further comprising:

d) a Data Memory; and

e) a Data Address Logic system,

said Data Address Logic system operative to control access to said Data Memory by said core processor, said Data Address Logic system also operative to control access to said Data Memory by said at least one off-core execution unit.

4. (Original) The data processor of claim 3, wherein said core processor is operative to retrieve said CLIW instruction from said CLIW memory, and said Data Address Logic system is operative to control access to said Data Memory by said core processor and to said Data Memory by said at least one off-core execution unit, substantially simultaneously.

5. (Original) The data processor of claim 3, further comprising:

f) a CLIW instruction decoder,

wherein said CLIW instruction decoder is operative to decode said CLIW instruction, and said Data Address Logic system is operative to control access to said Data Memory by said core processor and to said Data Memory by said at least one off-core execution unit, substantially simultaneously.

6. (Original) A method for processing data comprising the steps of:

~~a) providing an off-core execution unit;~~

[[b]]a) providing a core processor; **[[and]]**

b) providing an off-core execution unit that is an external off-core processing unit connected to said core processor in an interchangeable and selectable manner by means of an interface; and

c) executing a CLIW instruction to process the data, by both said core processor and said off-core execution unit.

7. (Original) The method of claim 6, wherein said off-core execution unit executes a respective portion of said CLIW instruction and said core processor executes a remainder of said CLIW instruction.

8. (Original) The method of claim 7, wherein said off-core execution unit executes only said respective portion of said CLIW instruction.

9. (Original) The method of claim 7, wherein said off-core execution unit executes said respective portion of said CLIW instruction simultaneously with execution by said core processor of said remainder of said CLIW instruction.

10. (Original) The method of claim 7, further comprising the steps of:

d) providing a CLIW memory;

e) storing said CLIW instruction in said CLIW memory;

f) retrieving said CLIW instruction from said CLIW memory, by said core processor; and

g) forwarding said respective portion of said CLIW instruction to said off-core execution unit, by said core processor, prior to said execution of said respective portion of said CLIW instruction by said off-core execution unit.

11. (Original) The method of claim 10, further comprising the step of:

h) issuing a reference instruction, by said core processor, to initiate said retrieving and executing of said CLIW instruction.

12. (Original) The method of claim 6, further comprising the steps of:

d) providing a data memory;

e) providing a data address logic system for controlling access to said data memory by said core processor and to said data memory by said

off-core execution unit; and

f) addressing data by said off-core execution unit and addressing data by said core processor under control of said data address logic system.

13. (Original) The method of claim 10, further comprising the steps of:

h) providing a data memory;

i) providing a data address logic system for controlling access to said data memory by said core processor and to said data memory by said off-core execution unit; and

j) addressing data by said off-core execution unit and addressing data by said core processor under control of said data address logic system;

and wherein said retrieving of said CLIW instruction from said CLIW memory is simultaneous with said addressing of data by said off-core execution unit and said addressing of data by said core processor.

14. (Original) The method of claim 13, further comprising the step of:

k) decoding said CLIW instruction,

and wherein said decoding of said CLIW instruction is simultaneous with said addressing of data by said off-core execution unit and said addressing of data by said core processor.

15-20. (Canceled)